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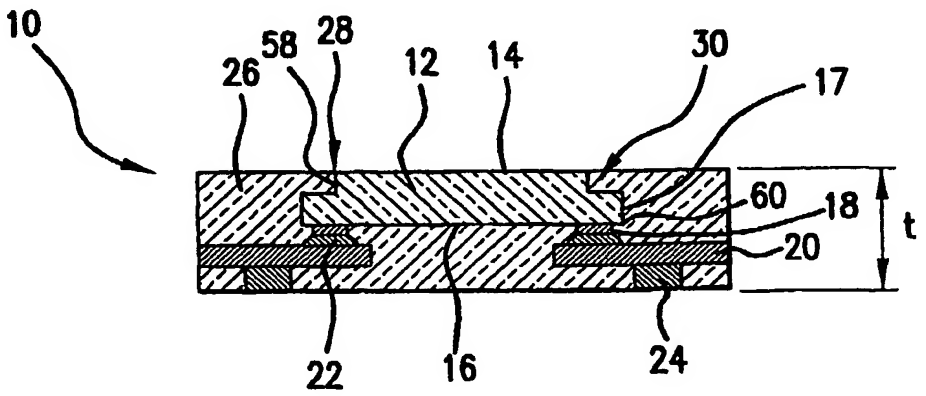
(54) Title: PACKAGE HAVING EXPOSED INTEGRATED CIRCUIT DEVICE



(57) Abstract: A package (10) includes an integrated circuit device (12) having an electrically active surface (16) and an opposing backside surface (14). A dielectric molding resin (26) at least partially encapsulates the integrated circuit die and the plurality of electrically conductive leads (20) with the backside surface (14) and the plurality of electrical contacts (24) being exposed on opposing sides of the package (10). Features (30) are formed into electrically inactive portions of the integrated circuit die (12) to seal moisture paths and relieve packaging stress. The features (30) are formed by forming a trough (54) partially through the backside (56) of the wafer (40) in alignment with a saw street (48), the trough (54) having a first width; and forming a channel (62) extending from the trough (54) to the electrically active face (42) to thereby singulate the integrated circuit device member, the channel (62) having a second width that is less than the first width. (Drawing Figure 2)

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— *with amended claims and statement*

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

AMENDED CLAIMS

[received by the International Bureau on 16 August 2004 (16.08.2004)
original claims2 and 8 amended; original claim 1 cancelled; remaining claims unchanged
(3 pages)]

2. An integrated circuit device package (10), comprising:

an integrated circuit device (12) having an electrically active surface (16) and an opposing backside surface (14) and sides (17) extending therebetween, said electrically active surface (16) having a plurality of electrically active circuit traces formed thereon and metallized bumps (18) extending from selected sites on said circuit traces;

a plurality of electrically conductive leads (20) each having respective first surfaces and opposing second surfaces;

a plurality of electrical contacts (24) extending outward from said respective first surfaces;

a solder (22) electrically and mechanically bonding said metallized bumps (18) to said second surfaces; and

a dielectric molding resin (26) formed into a package at least partially encapsulating said integrated circuit device (12) and said plurality of electrically conductive leads (20), said sides (17) are covered by said dielectric molding resin (26), and said backside surface (14) and said plurality of electrical contacts (24) are exposed on opposing sides of said package, wherein said sides (17) include at least one feature that is effective to limit the ingress of moisture along an interface between said integrated circuit device (12) and said dielectric molding resin (26).

3. The package (10) of claim 2 wherein said at least one feature includes two elements (58, 60) that intersect at an angle of approximately 90°.

4. The package (10) of claim 2 wherein a thickness of said package (10) is less than three times a thickness of said integrated circuit device (12).

5. The package (10) of claim 4 wherein said thickness of said package (10) is approximately 0.01 inch.

6. The package (10) of claim 2 wherein said integrated circuit device (12) is a sensor responsive to external stimulus.

7. The package (10) of claim 6 wherein said external stimulus is a touch.

8. A method for packaging an integrated circuit device member, the method comprising:

a) providing a wafer (40) containing a matrix of integrated circuit device members (44), each one of said integrated circuit device members (44) having a respective electrically active face (42) and an opposing backside (56), and a saw street (48) circumscribing each one of said integrated circuit members (44);

b) forming a trough (54) partially through said backside (56) of said wafer (40) in alignment with said saw street (48), said trough (54) having a first width;

c) forming a channel (62) extending from said trough (54) to said electrically active face (54) to thereby singulate said integrated circuit device member (44), said channel (62) having a second width that is less than said first width such that a portion of said trough (54) forms a step feature (30) circumscribing said integrated circuit device member (44) after singulation; and

d) encapsulating at least a portion of said integrated circuit device member (44) in a dielectric molding resin (26) to form a package (10) wherein at least a portion of said backside (56) is exposed from said package (10) and said dielectric molding resin (26) covers said step feature (30).

9. The method of claim 8 wherein prior to step (b), said electrically active face (54) is non-permanently bonded to a first electrically non-conductive substrate (50).

10. The method of claim 9 wherein said non-permanent bonding is by an adhesive.

11. The method of claim 10 wherein said first non-conductive substrate (50) is selected to be a polymer-backed tape.

12. The method of claim 9 wherein said troughs (54) are formed to have sidewalls (58) and a base (60) with a depth of from 30% to 70% of the thickness of said integrated circuit device member (44).

13. The method of claim 12 wherein said sidewalls (58) and said base (60) are formed to intersect at an angle of approximately 90°.

AMENDED SHEET (ARTICLE 19)

14. The method of claim 13 wherein said channel (62) is formed beginning at said base (60).

15. The method of claim 12 wherein prior to step (c), said wafer (40) is removed from said first non-conductive substrate (50), flipped and attached to a second non-conductive substrate with said backside (56) contacting said non-conductive substrate (50).

16. The method of claim 15 wherein said channel (62) is formed beginning at said saw street (48).

17. The method of claim 14 wherein following singulation said integrated circuit device (44) is removed from said non-conductive substrate (50) by a die/chip bonding pick and place machine.

18. The method of claim 17 wherein said thin wafer (40) has been back-ground to a thickness of 25 microns or less.

19. The method of claim 8, further comprising:

providing a plurality of electrically conductive leads (20) each having respective first surfaces and opposing second surfaces;

providing a plurality of electrical contacts (24) extending outward from said respective first surfaces;

before step (d), electrically bonding portions of said electrically active face (42) of said integrated circuit device member (44) with said second surfaces of said electrically conductive leads (20); and

wherein step (d) further includes encapsulating at least a portion of said electrically conductive leads (20) and said electrical contacts (24) in said dielectric molding resin (26) such that a portion of each electrical contact in said plurality of electrical contacts (24) is exposed from said dielectric molding resin (26).

AMENDED SHEET (ARTICLE 19)

STATEMENT UNDER ARTICLE 19 (1)

In the International Search Report, claims 1-3 were indicated as not being novel or not involving an inventive step in view of U.S. Patent No. 6,326,701 to Shinogi et al. (Shinogi et al.). Similarly, claims 4-7 were indicated as not involving an inventive step in view of Shinogi et al. when combined with one or more other such documents. Shinogi et al. discloses a chip size package wherein a removal area EL is provided as a first dicing line in a dicing area, coat materials 6' and 7' are put on the flanks of the removal area, a resin layer R is formed, and a dicing blade narrower than the width of the removal area EL is used to fully cut on a second dicing line. As shown in Shinogi et al. (e.g., FIG. 5), the sides of the semiconductor substrate are exposed after dicing. In contrast, Applicant's amended claim 2 (from which claims 3-7 depend) recites an integrated circuit device package wherein, *inter alia*, sides of an integrated circuit device are covered by a dielectric molding resin, and wherein the sides include at least one feature that is effective to limit the ingress of moisture along an interface between said integrated circuit device and the dielectric molding resin.

In the International Search Report, claims 8-18 were indicated as not being novel or not involving an inventive step in view of U.S. Patent No. 6,580,152 to Hasegawa (Hasegawa). Hasegawa discloses a semiconductor device wherein the semiconductor substrate has an exposed, steplike section that provides a surface for visual inspection when the semiconductor device is attached to the printed circuit board. In contrast, Applicant's claims 8-18 are directed to a method wherein the dielectric molding resin covers a step feature formed on the backside of the integrated circuit device member. As described in Applicant's specification at pages 5 and 6, the step feature prevents the ingress of moisture into the package 10 along the interface between the integrated circuit device and the molding resin, and mechanically locks the integrated circuit device to the molding resin.

In the International Search Report, claims 1-7 were indicated as not involving an inventive step in view of U.S. Patent No. 6,107,164 to Ohuchi (Ohuchi) when combined with

one or more other such documents. However, Ohuchi does not discuss at least one feature that is effective to limit the ingress of moisture along an interface between the integrated circuit device and the dielectric molding resin, as recited in Applicant's amended claim 2.